fifth instructions for performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

A4 Cont

sixth instructions for writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

REMARKS

Claims 1-32 are pending in the present application. Claims 1, 12, 17, 18, 19, and 30 have been amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation

The examiner has rejected claims 1-6, 12-24 and 30 under 35 U.S.C. § 102(b) as being anticipated by *Noorbakhsh* (5,699,498). This rejection is respectfully traversed.

In rejecting the claims, the examiner stated:

> *Noorbakhsh* teaches a video graphics array controllers with bit boundary block transfer engines or hardware accelerators (Fig. 1) comprising a system memory (14) for storing source bitmap (col. 1, lines 31-35), a video memory (22) for storing destination bitmap (36-37), a host processor (12), a system bus (16), and a graphics controller (20) for performing a raster operation of the source and destination bitmap (col. 1, lines 24-30); and writing the resulted into the video memory (col. 1, lines 30-31). Therefore, at least claims 1-6, 12-24 and 30 are anticipated by *Noorbakhsh*.

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A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process

a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

In this particular case, each and every feature of the presently claimed invention is not shown in the same arrangement in *Noorbakhsh* as in claim 1 in its amended form. Specifically, amended claim 1 reads as follows:

> 1. A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:
>
> selecting a first plurality of picture elements from the system memory;
>
> selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;
>
> reading the first plurality of picture elements from the system memory;
>
> reading the second plurality of picture elements from the video memory;
>
> performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and
>
> writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

Independent claims 12, 19, and 30 contain similar features.

The portions of *Noorbakhsh* cited by the examiner teach a general raster operation, not the steps of the presently claimed invention in amended claim 1. First, Figure 1 of *Noorbakhsh* is as follows:

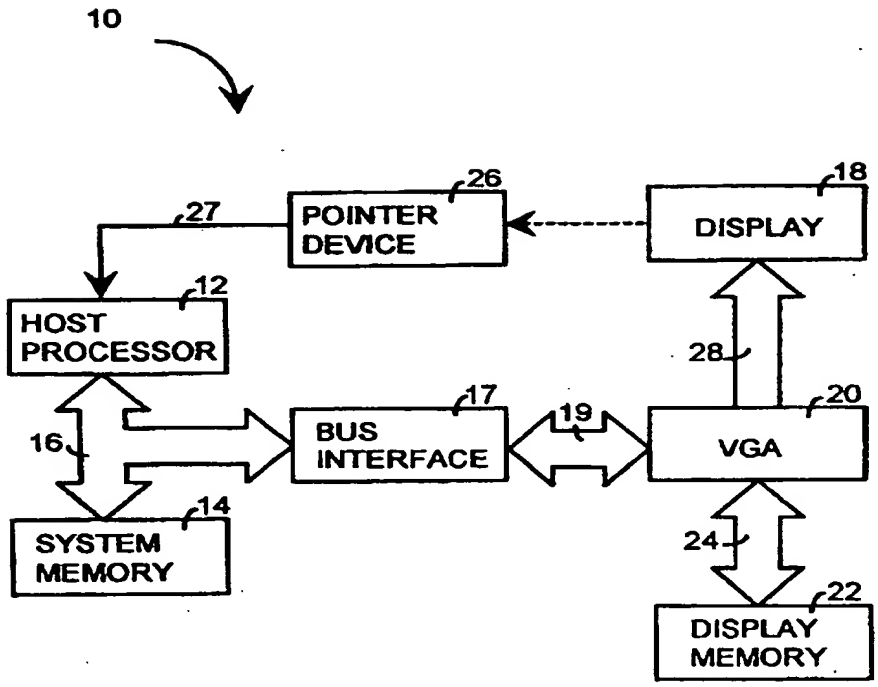

fig.1

As can be seen, Figure 1 of *Noorbakhsh* only discloses components used in displaying data. Nowhere does this figure teach the steps of the presently claimed invention in amended claim 1. Next, the examiner cites to the following section of *Noorbakhsh* for performing a raster operation of the source and destination bitmap and for routing the results into a video memory:

> More particularly, a BitBLT operation comprises a sequence of steps including reading data from a source memory area and data from a destination memory area, logically combining the data respectively read from the source memory area and the destination memory area using one of a number of logical operations generally referred to as raster operations ("ROPs"), and writing the result of the logical operation into the destination memory area.

Noorbakhsh, col. 1, lines 24-31. As can be seen, this portion of *Noorbakhsh* teaches combining data and performing a raster operation. The data is then written back into a destination memory area. This cited section of *Noorbakhsh*,

however, fails to teach selecting the plurality of process picture elements to the video memory such that the direction of data on the bus is minimized between the reading and writing of the picture elements. This particular feature is not shown in *Noorbakhsh*. The minimizing of changes in the direction of data on a bus through a selection of picture elements in amended claim 1 provides improved performance in processing graphics data. This feature is not found in *Noorbakhsh*.

Therefore, each and every feature of the presently claimed invention is not shown in *Noorbakhsh* in the same arrangement as in claim 1. As a result, *Noorbakhsh* does not anticipate claim 1. Consequently, the other independent claims having features similar to claim 1 also are patentable over *Noorbakhsh*. In addition, the dependent claims depend from one of the independent claims and are patentable over the cited reference for the same reason. Further, these claims include other features not shown in *Noorbakhsh*. For example, the portions of *Noorbakhsh* cited by the examiner do not teach that the process picture elements form a scan line as recited in claim 2. The sections cited by the examiner are general descriptions of a computer system and a process for performing a bit boundary block transfer.

Therefore, the rejection of claims 1-6, 12-24 and 30 under 35 U.S.C. § 102(b) has been overcome.

Further, no teaching, suggestion, or incentive is present in this reference to modify *Noorbakhsh* to select the process picture elements in a manner such that the direction of data on the bus is minimized between the reading and the writing of the picture elements from the different memories. The mere fact that *Noorbakhsh* could be modified to include such a feature does not make such a modification obvious.

Importantly, one of ordinary skill in the art would not be motivated to make such a modification when this reference is considered as a whole for what it teaches, rather than in a piecemeal fashion. *Noorbakhsh* is directed towards reducing the size of integrated circuits. In doing so, *Noorbakhsh* teaches the following:

These and additional objects are accomplished by the various aspects of the present invention, wherein briefly stated, one aspect of the invention is a controller connected to a memory storing red, green, and blue color data for individual pixels of a display screen. Included in the controller are: means for storing data indicative of predefined shades of red, green, and blue; means for receiving monochrome color data for indicated pixels of the display screen; means for receiving red, green, and blue color data from the memory, for the indicated pixels of the display screen; means for logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and means for generating a plurality of column address strobe signals from the received monochrome color data such that the generated plurality of column address strobe signals cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Another aspect of the invention is a method of performing a BitBLT operation on indicated pixels of a display screen, comprising: receiving data indicative of predefined shades of red, green, and blue; receiving monochrome color data for the indicated pixels of the display screen; receiving red, green, and blue color data from a memory, for the indicated pixels of the display screen; logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and generating a plurality of column address strobe signals from the received monochrome color data such that the generated plurality of column address strobe signals cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Still another aspect of the invention is a computer system comprising: a host processor; a display having a display screen with a number of pixels; a memory storing red, green, and blue color data for individual pixels of the display screen; and a controller. Included in the controller are: means for storing data indicative of predefined shades of red, green, and blue; means for receiving monochrome color data for indicated pixels of the display screen; means for receiving red, green, and blue color data from the memory, for the indicated pixels of the display screen, means for logically combining the received color data and corresponding ones of the predefined shades of red, green, and blue; and means for generating a plurality of column address strobes from the received monochrome data such that the generated plurality of column address strobes cause the logically combined color data to replace stored red, green, and blue color data in the memory for selected ones of the indicated pixels as determined by the monochrome color data.

Noorbakhsh col. 7, line 56 – col. 8, line 40. As can be seen, *Noorbakhsh* does not teach, suggest, or provide a motivation for a feature in which data from a system memory and video memory are selected for processing such that changes in the direction of the data on the bus are minimized between the reading and writing of the picture elements. Therefore, the presently claimed invention in the rejected claims can be reached only through an improper use of hindsight with the benefit of applicants' invention as a template for the needed changes.

II. 35 U.S.C. § 103, Obviousness

The examiner has rejected claims 7-11, 25-29 and 31-32 under 35 U.S.C. § 103(a) as being unpatentable over *Noorbakhsh* (5,699,498) in view of *Brech* (5,790,887). This rejection is respectfully traversed.

In rejecting the claims, the examiner stated the following:

> The teachings of *Noorbakhsh* are given in previous paragraph of this office action. However, *Noorbakhsh* fails to explicitly suggest or teach collecting a set of I/O operations into a batch of I/O operations... This is what *Brech* teaches (abstract). *Brech* teaches a batched list of PIO operations is stored in a buffer. Then the batched list of PIO operations is moved as a **single system bus operation** to an I/O bus interface unit. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of *Brech* into the system of *Noorbakhsh* in order to avoid the processor wait time and inefficient bus usage problems amount prior art system as taught by *Brech* (col. 1, lines 13-67). Therefore, at least claims 7-11, 25-29 and 31-32 would have been obvious.

Office Action dated April 5, 2002, page 3.

A. The examiner bears the burden of establishing a *prima facie* case of obviousness.

The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). In this particular case, the examiner has failed to establish a *prima facie* of obviousness

based on the prior art because the examiner has failed to consider all of the claim features recited in the claims and because the examiner has failed to properly combine the references. These reasons are described in more detail below.

B. All claim limitations must be considered, especially when missing from prior art.

Additionally, in comparing *Noorbakhsh* and *Brech* to the claimed invention, the claimed features of the presently claimed invention may not be ignored in an obviousness to determination. The present invention in claim 7 recites:

> 7. A method for performing raster operations in a graphics system, wherein the method comprises the data processing system implemented steps of:
>
> collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display; and
>
> sending the set of input operations on a video bus in a single operation.

Independent claims 25 and 31 contain similar features. In this particular case, the examiner has failed to consider that the input operations are collected into a batch of input operations substantially equal to a number of rasters and a video display. The examiner has failed to take this particular feature into account in combining *Noorbakhsh* with *Brech*. Therefore, a combination of *Noorbakhsh* and *Brech* even if proper would not reach the presently claimed invention.

C. Stating that it is obvious to try or make a modification or combination without a suggestion in the prior art is not *prima facie* obviousness.

The mere fact that a prior art reference can be readily modified does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Laskowski*, 871 F.2d 115, 10 U.S.P.Q.2d 1397 (Fed. Cir. 1989) and also *see In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992) and *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1993). The examiner may not merely state that the

modification would have been obvious to one of ordinary skill in the art without pointing out in the prior art a suggestion of the desirability of the proposed modification. The mere fact that the examiner could modify *Brech* to collect the input operations into a batch of input operations substantially equal to a number of rasters in a video display does not make such a modification obvious. The modification cannot be made without some teaching, suggestion, or incentive for this particular modification. The sections cited by the examiner provide no such teaching, suggestion, or incentive. Instead, these sections have only been cited for the proposition that a batch list of operations are moved as a single bus operation. The examiner has not pointed out any teaching, suggestion, or incentive for collecting a set of input operations into a batch of input operations substantially equal to a number of rasters in a video display and then sending that set of input operations on a video bus in a single operation. Therefore, a *prima facie* case of obviousness has not been made with respect to *Brech*. Further, *Noorbakhsh* also provides no teaching, suggestion, or incentive for such a modification. As a result, a combination of these two references, even if proper, would not reach the presently claimed invention.

D. A proper prima facie case of obviousness must be supported by some teaching or suggestion contained in the prior art.

A proper *prima facie* case of obviousness must be supported by some teaching or suggestion contained in the combined references. Applicants respectfully submit that the references cited cannot be combined to produce the claimed invention. The rule is:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some **teaching, suggestion** or **incentive** supporting the combination.

In re Geiger, 815 F.2d 686, 688, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987)(emphasis added). In this case, no teaching, suggestion, or incentive has been given for combining these two references as proposed by the examiner. The examiner has only stated that it would be obvious to combine these to avoid processor wait time and inefficient bus usage problems in the prior art system taught by *Brech*.

Brech, in the cited section, is directed towards processing input/output operations in a computer system. *Noorbakhsh*, however, is not concerned with such a problem. Instead, *Noorbakhsh* is more concerned with the following:

> In designing integrated circuits, it is an ongoing design goal to reduce the size of integrated circuits providing a given functionality. It is especially desirable to achieve such size reduction by reducing the complexity (or number of transistors) of the integrated circuitry performing the function or a comparable function.

Noorbakhsh col. 7, lines 40-45. As can be seen, when viewed by one of ordinary skill in the art, *Noorbakhsh* is more concerned with reducing the size of integrated circuits providing a particular functionality, rather than with problems associated with bus usage. Therefore, one of ordinary skill in the art would not be motivated to combine the teachings in these two references when they are considered as a whole.

Importantly, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780, 1784 (Fed. Cir. 1992). One of ordinary skill in the art would consider the problems addressed by a reference to determine whether some teaching, suggestion, or incentive is present to support a combination.

In this particular case, the problems addressed by each of the references are different as well as the solutions. For example, *Noorbakhsh* is directed towards a VGA controller in a computer system described as follows:

> A computer system includes a host processor, a system memory, a display unit, a pointer device, a VGA controller, and a display memory. The VGA controller communicates with the display memory through an 8-byte wide data bus such that each byte is controlled by a separate column address strobe. To perform a BitBLT operation on a monochrome pattern to be logically combined with 888-RGB color-space formatted data in the display memory, the VGA controller includes a BitBLT control for generating numerous control signals; a color expand circuit for generating in response to such control signals, an 8-byte wide pattern of 888-RGB color-space formatted foreground color data; a circuit for logically combining in response to such control signals, the 8-byte wide pattern of 888-RGB color-space formatted foreground color data and a corresponding 8-byte wide pattern of 888-RGB color-space data received

from the 8-byte wide data bus; a bit align circuit for generating in response to such control signals, column address strobe values indicative of bits of the monochrome pattern corresponding to the 8-byte wide pattern of 888-RGB color-space data received from the data bus, by bit aligning the bits of the monochrome pattern; and a memory sequencer for generating in response to such control signals, column address strobe signals corresponding to the values received from the bit align circuit, for strobing into the display memory selected bytes of the logically combined 8-bytes of data.

On the other hand, *Brech* is more concerned with a method and apparatus for processing program input/output operations described as follows:

> A method and apparatus are provided for processing programmed input/output (PIO) operations in a computer system. A batched list of PIO operations is stored in a buffer. Then the batched list of PIO operations is moved as a single system bus operation to an I/O bus interface unit. The I/O bus interface unit includes sequencer logic. The sequencer logic is used for executing the batched list of PIO operations and for providing an ordered sequence of PIO operations to a system I/O bus. The method and apparatus of the invention enhances the use of non-intelligent I/O adapters in a computer system by reducing the overhead of system PIO operations. Also the correctly ordered sequence of PIO commands provided by the sequencer logic facilitates the use of non-intelligent I/O adapters in reduced instruction-set computer (RISC) systems.

Brech, Abstract. As can be seen, when these two references are considered as a whole for what they teach one of ordinary skill in the art, no teaching, suggestion, or incentive is present to support the combination.

Therefore, independent claim 7 and the other independent claims rejected are patentable over these references. Thus, these references cannot be combined absent an improper use of hindsight with the benefit of applicants' invention as a template to piece together the prior art.

In addition, the other claims rejected in this section are dependent claims depending from one of the independent claims. For example, claim 8 collects output operations into a batch of output operations substantially equal to a number of raster operations and sends them to a video bus in a single operation. These features are not shown or suggested in *Brech*. As a result, these claims are

patentable over the two cited references for the same reasons. Further, these claims include other additional features not suggested by these references.

III. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 6/20/02

Respectfully submitted,

Duke W. Yee
Reg. No. 34,285
Carstens, Yee & Cahoon, LLP
P.O. Box 802334
Dallas, TX 75380
(972) 367-2001
Attorney for Applicants

APPENDIX OF AMENDED CLAIMS

1. (Amended) A method in a data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the method comprising the data processing system implemented steps of:

[reading] selecting a first plurality of picture elements from the system memory;

[reading] selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading the first plurality of picture elements from the system memory;

reading the second plurality of picture elements from the video memory;

performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

writing the plurality of processed picture elements to the video memory [such that], wherein changes in the direction of data on the bus [is]are [unchanged] minimized between the reading and writing of picture elements.

12. (Amended) A data processing system comprising:

a bus;

a system memory connected the bus, wherein a first plurality of graphics elements are located within the system memory;

a video memory connected to the bus, wherein a second plurality of graphics elements are located within the video memory;

a processor unit connected to the bus, wherein the processor unit executes instructions [for an operating system, wherein the operating system reads the second plurality of graphics elements within the video memory into the system memory, performs a raster operation on the second plurality of graphics elements within the video memory with the second plurality of graphics elements within the system memory to form a plurality of processed graphics elements, and writes the plurality of processed graphics elements into the video memory, wherein the first plurality and the second plurality form a set of pluralities and between the first plurality and the second plurality, at least one of the pluralities is transferred in a single operation] to select a first plurality of picture elements from the system memory; select a second plurality of picture elements from the video memory in which the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements; read the first plurality of picture elements from the system memory; read the second plurality of picture elements from the video memory; perform a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and write the plurality of processed picture elements to the video memory in which changes in the direction of data on the bus are minimized between the reading and writing of picture elements.

17. (Amended) The data processing system of claim 12, wherein a graphics engine [in the operating system] performs the raster operation.

18. (Amended) The data processing system of claim 12, wherein a video driver [in the operating system] performs the raster operation.

19. (Amended) A data processing system for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and

wherein the graphics data is organized into picture elements, the data processing system comprising:

first [reading]selecting means for [reading]selecting a first plurality of picture elements from the system memory;

second [reading]selecting means for [reading]selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

reading means for reading the first plurality of picture elements from the system memory;

reading means for reading the second plurality of picture elements from the video memory;

performing means for performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

writing means for writing the plurality of processed picture elements to the video memory [such that], wherein changes in the direction of data on the bus [is]are [unchanged]minimized between the reading and writing of picture elements.

30. (Amended) A computer program product in a computer readable medium for performing a raster operation of graphics data, wherein the data processing system includes a system memory and a video memory, wherein the system memory and the video memory are connected by a bus and wherein the graphics data is organized into picture elements, the computer program product comprising:

first instructions for [reading]selecting a first plurality of picture elements from the system memory;

second instructions for [reading]selecting a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the

bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements;

third instructions for reading the first of a first plurality of picture elements from the system memory;

fourth instructions for reading the second plurality of picture elements from the video memory;

[third]fifth instructions for performing a raster operation on the first plurality of picture elements and the second plurality of picture elements to form a plurality of processed picture elements; and

[fourth]sixth instructions for writing the plurality of processed picture elements to the video memory, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements.